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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,911	03/28/2001	Satoshi Katoh	NE203-US	2416

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EXAMINER

COUSO, YON JUNG

ART UNIT	PAPER NUMBER
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2625

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/818,911 ✓

Applicant(s)

KATOH, SATOSHI

Examiner

Yon Couso

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 April 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2 and 4-24 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 14-24 is/are allowed.
6) ☒ Claim(s) 1, 2, 4-13 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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1. Applicant's arguments filed April 15, 2005 have been fully considered but they are not persuasive.

a. The applicant argues that the Nagano teaches the use of two AD converters 51 and 42, and so requires a selector 53 to select the output from one of the two AD converters. The applicant therefore concludes that the claim 1 is patentably distinct from the Nagano reference. The examiner disagrees. Figure 4 (prior art) in the Nagano reference discloses a single AD converter (42) that does not require a selector. Moreover, turning to the applicant's drawings, figure 5 discloses second embodiment, which is a variation from the first embodiment. A single AD converter is replaced with three AD converters and a selector (20-23 in figure 5). The Nagano reference and the applicant's disclosure make it very clear that replacing a single AD converter with a plural AD converters with a selector is common practice in the art. Moreover, Nagano already discloses image sensing apparatus with a single AD converter (42 in figure 4).

b. Thank you for correctly pointing out the allowed claims. Claims 14-24 are allowed.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 and 4 are rejected under 35 U.S.C. § 102(b) as being anticipated by Nagano, 5,687,003.

The arguments advanced in paragraph 1 above as to the applicability of the reference are incorporated herein.

For claim 1, an image sensing apparatus comprising: an image quality mode setting block for setting only one of a plurality of image quality modes is provided by Nagano in at least Fig. 1, block 52, and the last full paragraph in c. 4; a solid state image sensing element for converting an optical image into an electric analog signal is provided by Nagano also in at least the last full paragraph in c. 4; and an A/D conversion block for converting the analog signal output from the solid state image sensing element into a digital signal with a quantization bit count corresponding only to the one image quality mode set by the image quality mode setting block also in the last full paragraph in c. 4, the first full paragraph in c. 5, and the third full paragraph in c. 6, as there is only one quality mode set at a time for selection of a corresponding bit count, of which bit count directly corresponds to only one of the A/D converters, which convert to digital with a quantization bit count corresponding only to the one quality mode. Nagano also discloses a single AD converter (42 in figure 4).

For claim 4, the image sensing apparatus as claimed in claim 1, wherein a higher image quality mode corresponds to a greater bit count and a lower image quality mode corresponds to a smaller bit count is provided by Nagano in at least the last full paragraph in c. 4, e.g. 12 bit and 8 bit counts.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the

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subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, as applied to claims 1 and 4 above, and in view of either JP08298601, Koji et al., as cited in the IDS, or JP401176119, Murakami.

For claim 2, the image sensing apparatus as claimed in claim 1, wherein the A/D conversion block comprises an A/D converter for selecting one of a plurality of quantization bit counts corresponding to the image quality mode is considered provided by Nagano where cited above, and by at least blocks 42, 51, and 53, where a specific bit count is clearly selected. While an A/D converter for selecting one of a quantization bit counts is considered provided by Nagano by at least blocks 51-53 and 42, because a quantization bit count is selected for an A/D converter, and an A/D converter is selected, either JP08298601 or JP401176119 provides for the same in at least the abstract of both. It would've been obvious to one having ordinary skill in the art at the time the invention was made to select one of a plurality of quantization bit counts corresponding to a mode for an A/D converter, since JP401176119 provides for reducing the power consumption, and JP08298601 provides for avoiding error and deterioration.

4. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, as applied to claims 1 and 4 above, and in view of Hasegawa et al., 5,384,645.

For claims 5 and 6, the image sensing apparatus as claimed in claim 1, further comprising a digital signal processing DSP block for performing image processing of the

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digital signal output from the AD conversion block, the DSP block having a quantization bit count corresponding to the image quality mode set by the image quality mode setting block, and wherein the digital signal processing block sets a corresponding quantization bit count when an image quality mode is set by the image quality mode setting block is almost implicit with Nagano, since Nagano provides for an image reader in the well known image processing systems as noted in c. 1, lines 10-14, which very commonly provide for at least one image processing function, and since such an image processor gets its input from the image sensing system of Nagao, such system would operate in accordance with the quantization bit count set by Nagano. In any case, Hasegawa explicitly teaches this in at least the second full paragraph in c. 3. Adapting the DSP, i.e. image processing, of Hasegawa with a different quantization bit count is exactly what Hasegawa teaches, and image processing is the next stage in the processing of Nagao, where Nagao outputs different quantization bit counts based on modes. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use a DSP for different quantization bit counts, since Hasegawa provides for at least the advantages of a decrease in circuitry heat and therefore a reduction in power consumption as well, improvement in processing speed, and without changing memory to process image data.

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5. Claims 7, 9-11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, and Hasegawa et al., 5,384,645, as applied to claims 5-6 above, and further in view of Nagai, 2001/0010561.

For claim 7, the image sensing apparatus as claimed in claim 5, further comprising a data thinning block for thinning the output signal from the digital signal processing DSP block is not explicitly provided by Nagano, but is conventional and well known, and is provided by Nagai in at least paragraphs 25-26 on page 2, which is provided after or to the output of the digital signal processing as claimed. It would've been obvious to one having ordinary skill in the art at the time the invention was made to thin the output of a DSP in processing, since this provides for at least fast processing.

For claims 9 and 13, the image sensing apparatus as claimed in claim 5, further comprising an image storage block for storing the output signal from the digital signal processing block as image data; and further comprising an image display block for displaying an image according to the output signal from the digital signal processing block, the image display block selecting whether to display the image during storage of image data in the image storage block is not explicitly provided by Nagano and Hasegawa, but is conventional and well known and is provided by the camera system of Nagai in at least paragraphs 32 and 37, where an image can be displayed or not and can be recorded in memory if desired. It would've been obvious to one having ordinary skill in the art at the time the invention was made to have the added feature of displaying or not while recording, since this can provide for saving power and also for selecting how the image is to be record as taught by Nagai.

For claim 10, the image sensing apparatus as claimed in claim 5, further comprising: an image storage block for storing the output signal from the digital signal processing block as image data; and an image display block for displaying the image according to the output signal from the digital signal processing block, wherein the solid state image sensing element, the AD conversion block, and the digital signal processing block stop operation while the image display block is displaying an image according to the image data stored in the image storage block, Nagai provides for storage from the DSP and displaying from the DSP, but does not explicitly recite stopping the operations.

However, since Nagai teaches playing back the images stored from memory (play back in paragraphs 45-50 and Fig. 5 as opposed to Fig. 4 picture taking mode), it inherently or clearly follows that the CCD, A/D converter, and DSP are not operating, since the image is not sensed unless in the picture taking mode and if the user presses the shutter-release in Fig. 4. Thus, if there is no image being sensed, then the CCD and all circuitry that come after it do not operate on a signal as claimed.

For claim 11, the image sensing apparatus as claimed in claim 1, wherein the image sensing apparatus comprises an electronic still camera is not explicitly provided by Nagano, but Nagano provides for the conventional and well known items of a camera including the well known optical sensor and A/D converters and output thereof. Nagai provides for an electronic still camera in at least the abstract. Nagai can use the A/D converters of Nagano with the electronic still camera of Nagai and vice versa. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use A/D converters with an electronic still camera, since the A/D

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converters provide for two optional modes for the advantage of speed and high resolution, and because the camera has the advantage of features modes including a zoom function, previewing the image, and image enhancement functions including at least gamma correction and color balancing.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, and Hasegawa et al., 5,384,645, and Nagai, 2001/0010561, as applied to claims 7, 9-11, and 13 above, and in view of Kubo et al., 6,639,626.

For claim 8, the image sensing apparatus as claimed in claim 7, wherein the digital signal processing block performs color interpolation processing is not explicitly provided by Nagai, but color interpolation is very typically used in an image signal processing circuit in a digital camera, such as that of Nagai noted above, where Nagai provides for "processing such as a gamma correction and color balance adjustment". Kubo provides for basically the same thing in a digital camera, but also clearly teaches color interpolation as well in at least Fig. 5, block 211a, Fig. 10, block 81, the last full paragraph in c. 13 and the paragraph bridging cols. 14-15, where the colors are RGB. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use color interpolation with at least the conventional and well known image signal processing of Nagai, since color interpolation is another conventional and well known image signal process, and because it and the other functions (gamma and color balancing) are common with Kubo and Nagai, and also provide for a higher fidelity image.

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7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, and Hasegawa et al., 5,384,645, and Nagai, 2001/0010561, as applied to claims 7, 9-11, and 13 above, and in view of JP 11-261871, Yoshihiro, as cited in the IDS.

For claim 10, see the rejection of at least claim 10 above without respect to Yoshihiro. Since claim 10 above is reasoned logically, Yoshihiro clearly teaches the idea of stopping operations clearly by cutting power to them, which can be used with at least Nagai for cutting power in the different modes and use power where only power is necessary. See the abstract of Yoshihiro. It would've been obvious to one having ordinary skill in the art at the time the invention was made to cut power to some circuits, since only certain circuits are needed for display as taught by Yoshihiro, which provides for the advantage of saving power, which is very advantageous in small low power digital still cameras.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, as applied to claims 1 and 4 above, and in view of Johnson et al., 6,686,957.

For claim 12, the image sensing apparatus as claimed in claim 1, wherein the A/D conversion block receives a bit count conversion signal from the image quality mode setting block, and converts the analog signal based on the bit count conversion signal can be considered provided by Nagano, since the data selector of Nagano in Fig. 1 can be considered part of the A/D conversion process. However, the A/D converters per se do not explicitly receive the quality mode. A/D converters per se receiving a quality mode is considered provided by Johnson in at least the first three full paragraphs

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in c. 8. Using the arrangement of Johnson can be used with the arrangement of Nagano by directly controlling the A/D converter, since either way – whether the A/D converters are directly controlled or not, Nagano would still provide for selecting a different bit count conversion as desired. It would've been obvious to one having ordinary skill in the art at the time the invention was made to control the A/D converter directly based on a quality mode setting signal as taught by Johnson with Nagano, since Johnson teaches at least “considerable power and battery savings” – same exact idea and purpose of Applicant.

9. Claims 14-24 are allowed.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

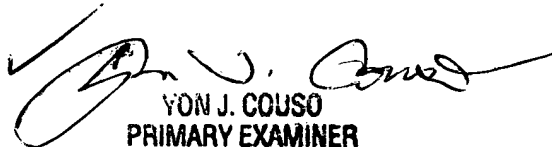
11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yon Couso whose telephone number is (571) 272-7448. The examiner can normally be reached on Monday through Friday from 8:30 to 5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta, can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YJC



YON J. COUSO
PRIMARY EXAMINER

June 17, 2005